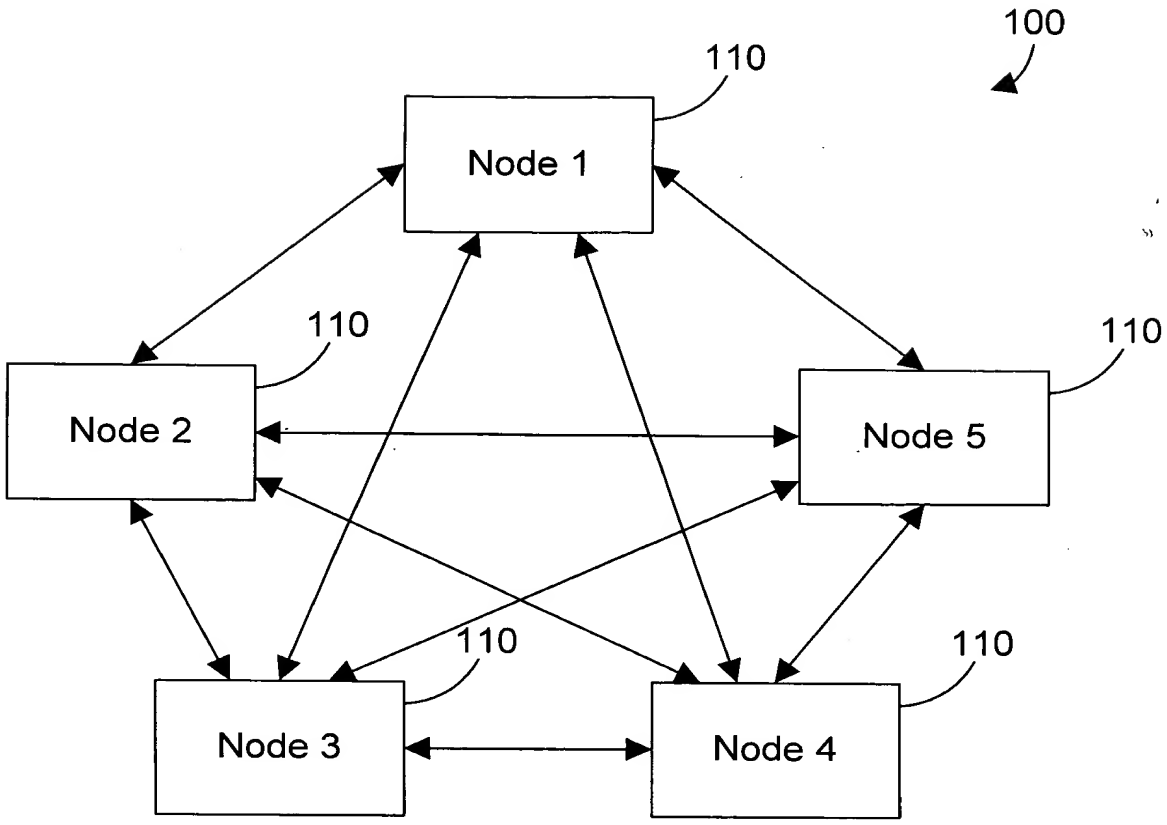


FIG. 1

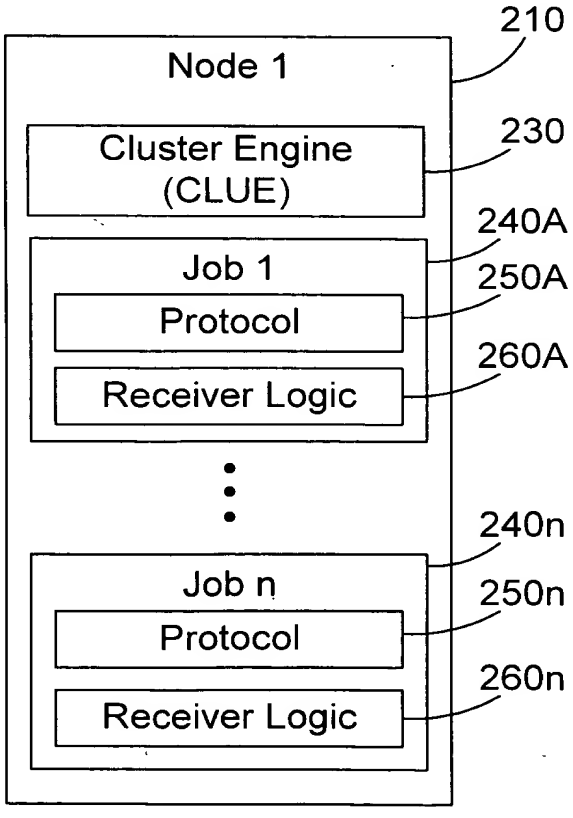


FIG. 2
Prior Art

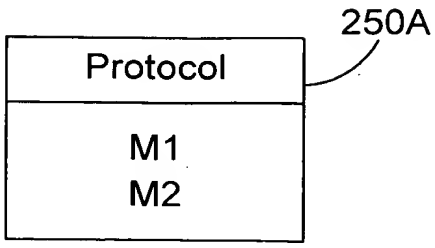


FIG. 3

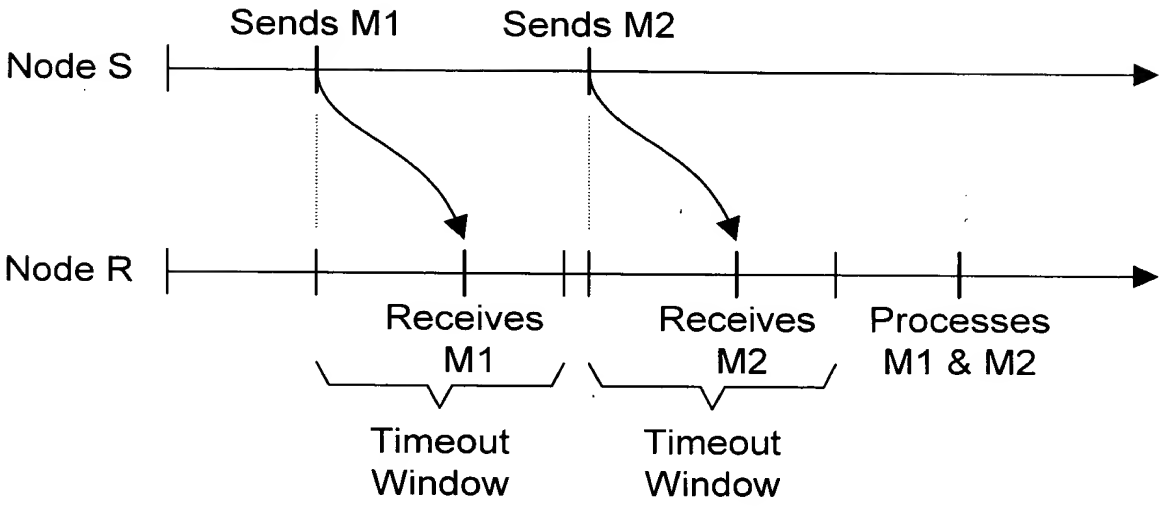


FIG. 4 Prior Art

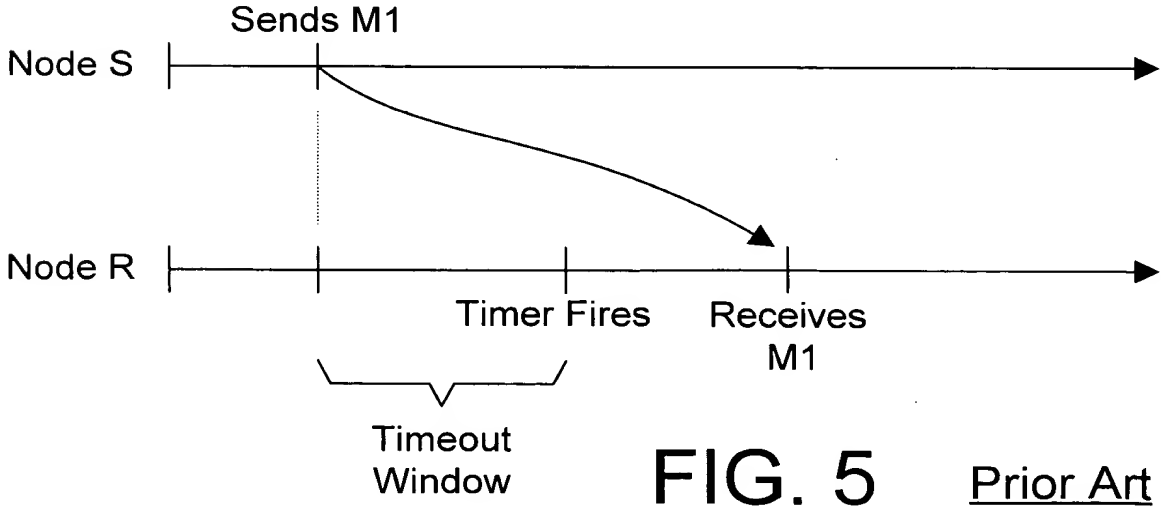


FIG. 5 Prior Art

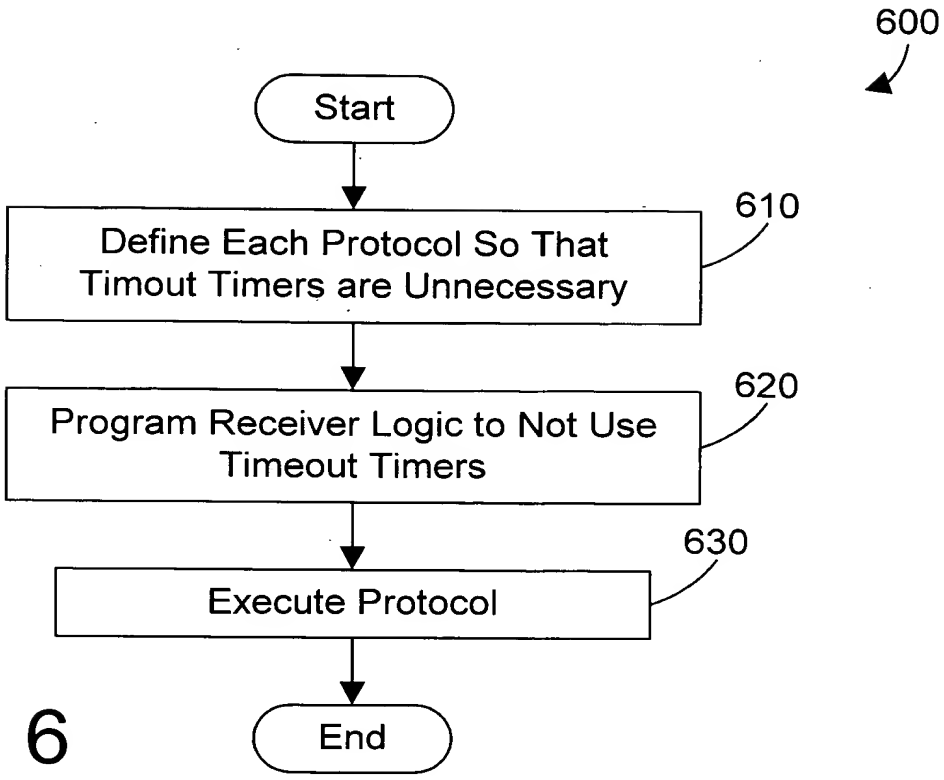
600
Start
Define Each Protocol So That Timout Timers are Unnecessary
610
Program Receiver Logic to Not Use Timeout Timers
620
Execute Protocol
630
End

FIG. 6

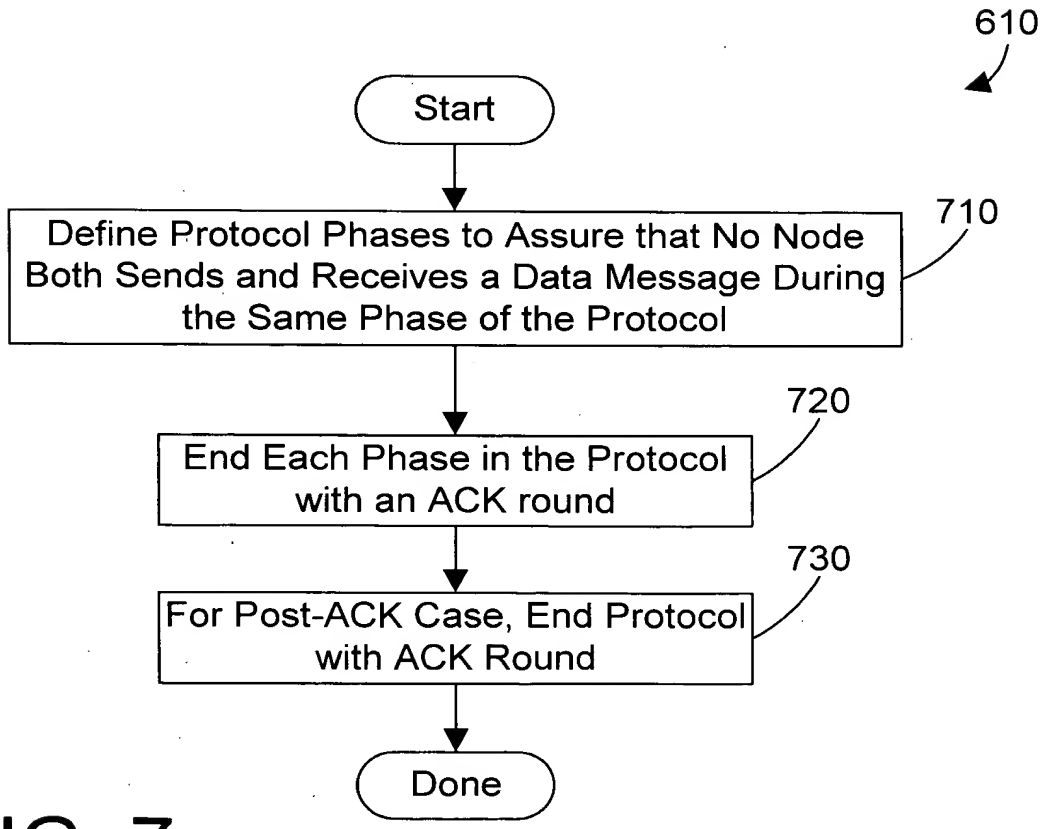
610
Start
Define Protocol Phases to Assure that No Node Both Sends and Receives a Data Message During the Same Phase of the Protocol
710
End Each Phase in the Protocol with an ACK round
720
For Post-ACK Case, End Protocol with ACK Round
730
Done

FIG. 7

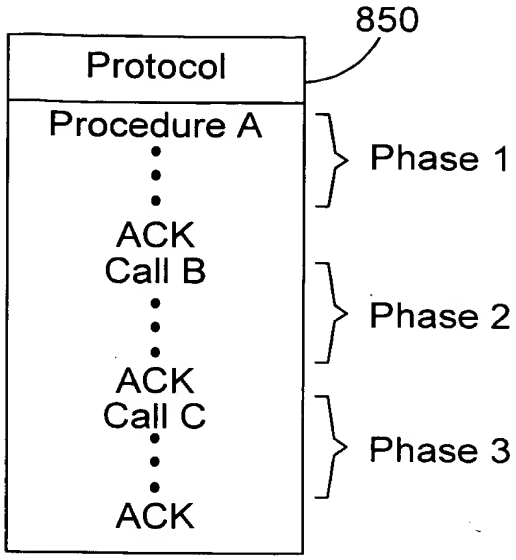


FIG. 8

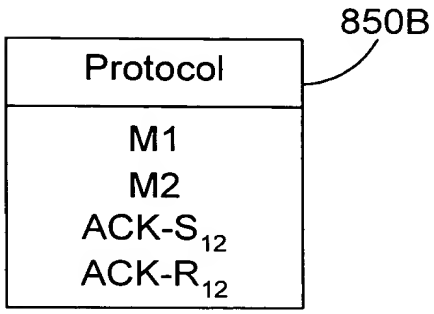


FIG. 9

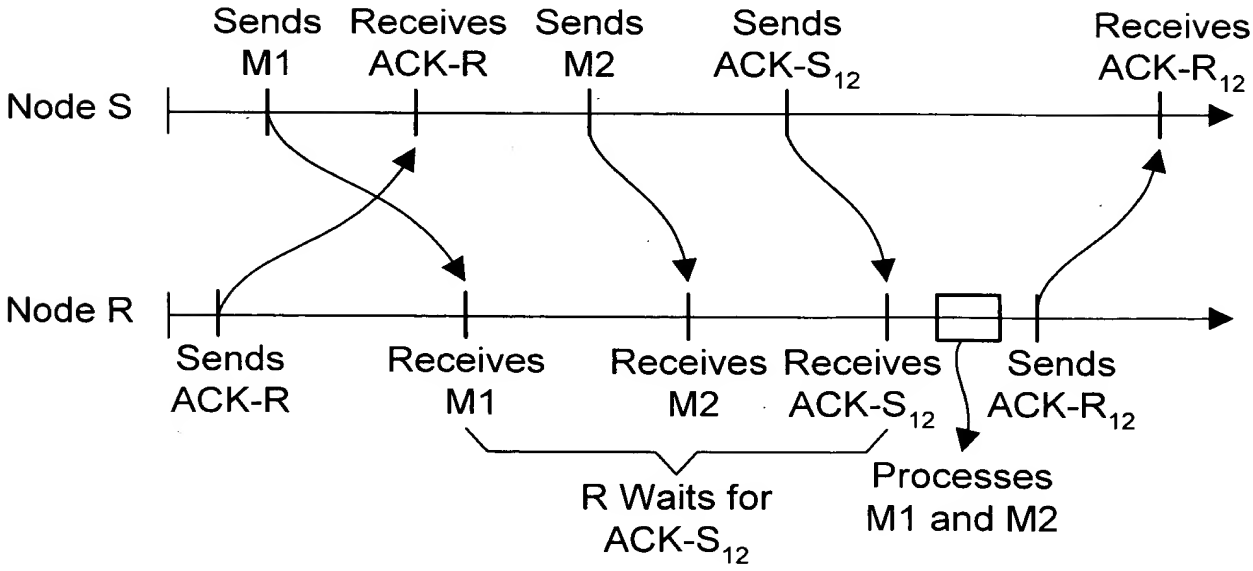


FIG. 10

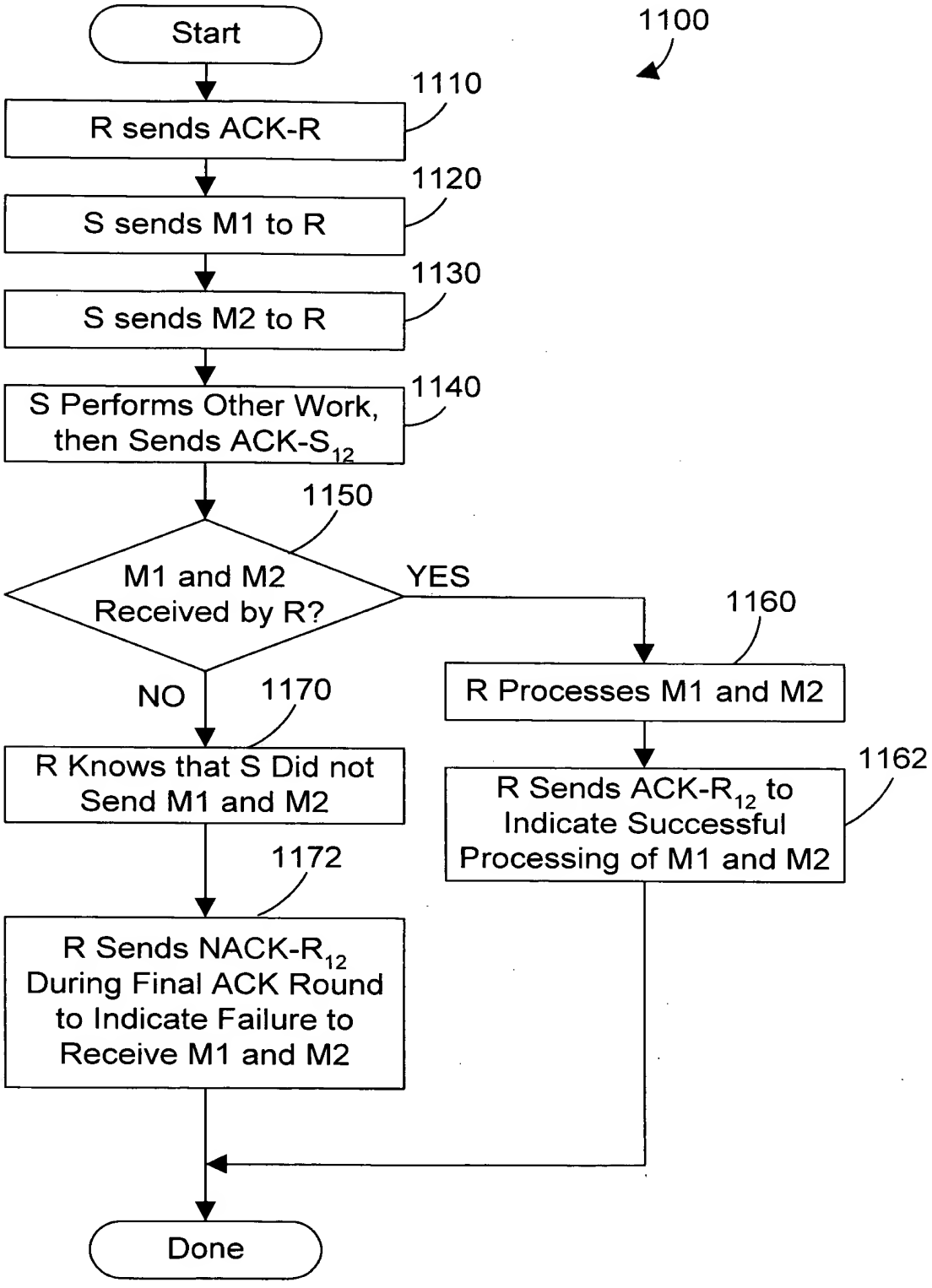
1100
Start
1110
R sends ACK-R
1120
S sends M1 to R
1130
S sends M2 to R
1140
S Performs Other Work, then Sends ACK-S12
1150
M1 and M2 Received by R?
YES
NO
1160
R Processes M1 and M2
1162
R Sends ACK-R12 to Indicate Successful Processing of M1 and M2
1170
R Knows that S Did not Send M1 and M2
1172
R Sends NACK-R12 During Final ACK Round to Indicate Failure to Receive M1 and M2
Done

FIG. 11

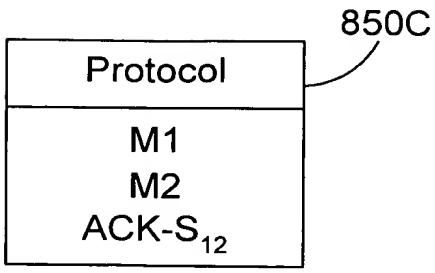
850C
Protocol
M1
M2
ACK-S12

FIG. 12

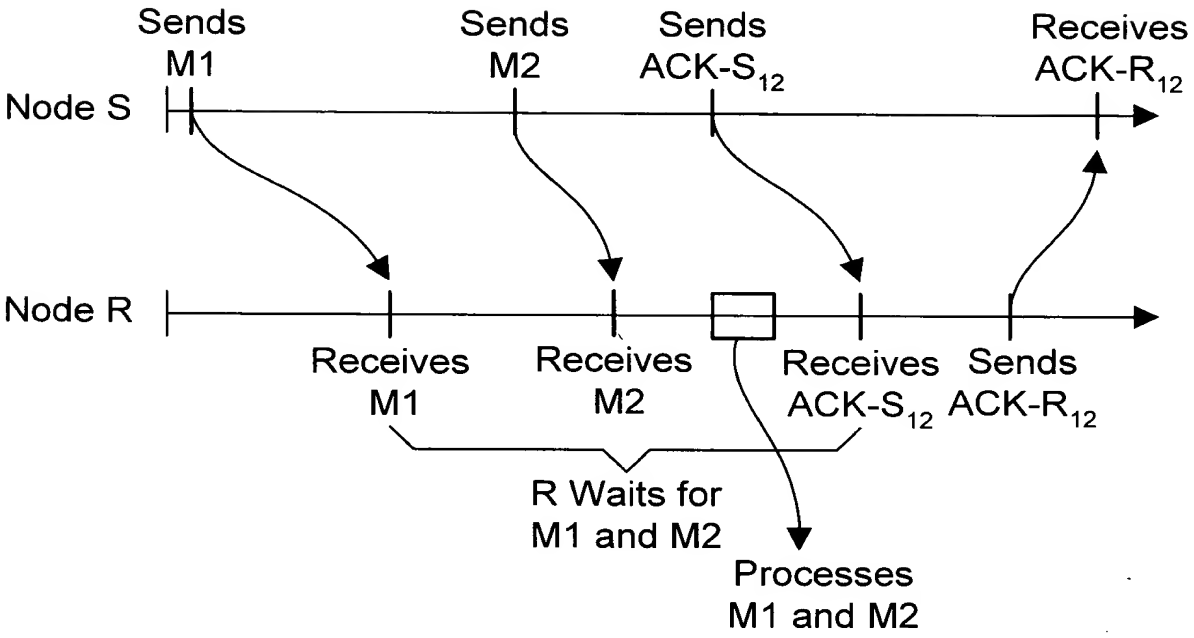
Sends M1
Sends M2
Sends ACK-S12
Receives ACK-R12
Node S
Node R
Receives M1
Receives M2
Receives ACK-S12
Sends ACK-R12
R Waits for M1 and M2
Processes M1 and M2

FIG. 13

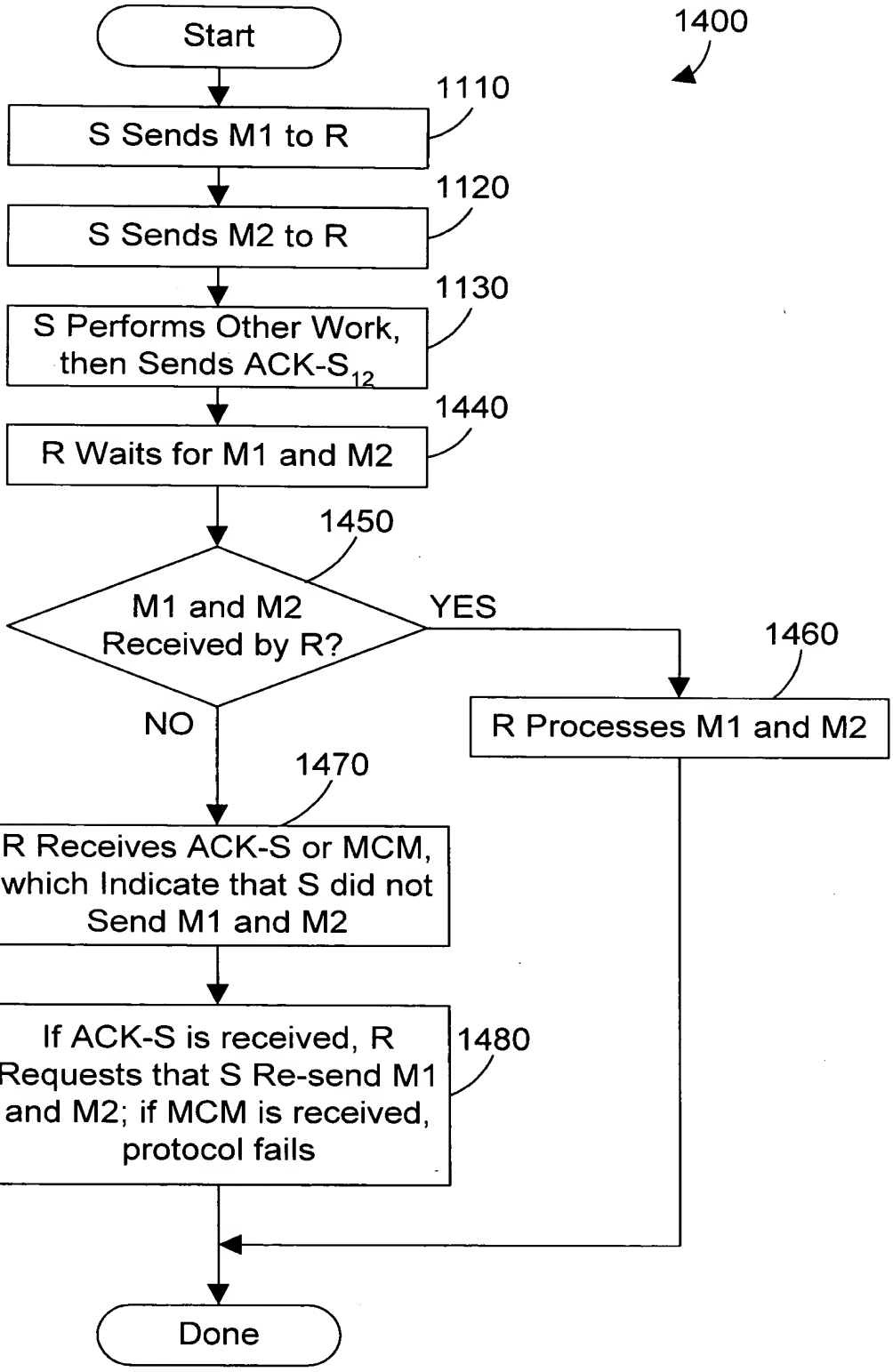
1400
Start
1110
S Sends M1 to R
1120
S Sends M2 to R
1130
S Performs Other Work, then Sends ACK-S12
1440
R Waits for M1 and M2
1450
M1 and M2 Received by R?
YES
NO
1460
R Processes M1 and M2
1470
R Receives ACK-S or MCM, which Indicate that S did not Send M1 and M2
If ACK-S is received, R Requests that S Re-send M1 and M2; if MCM is received, protocol fails
1480
Done

FIG. 14

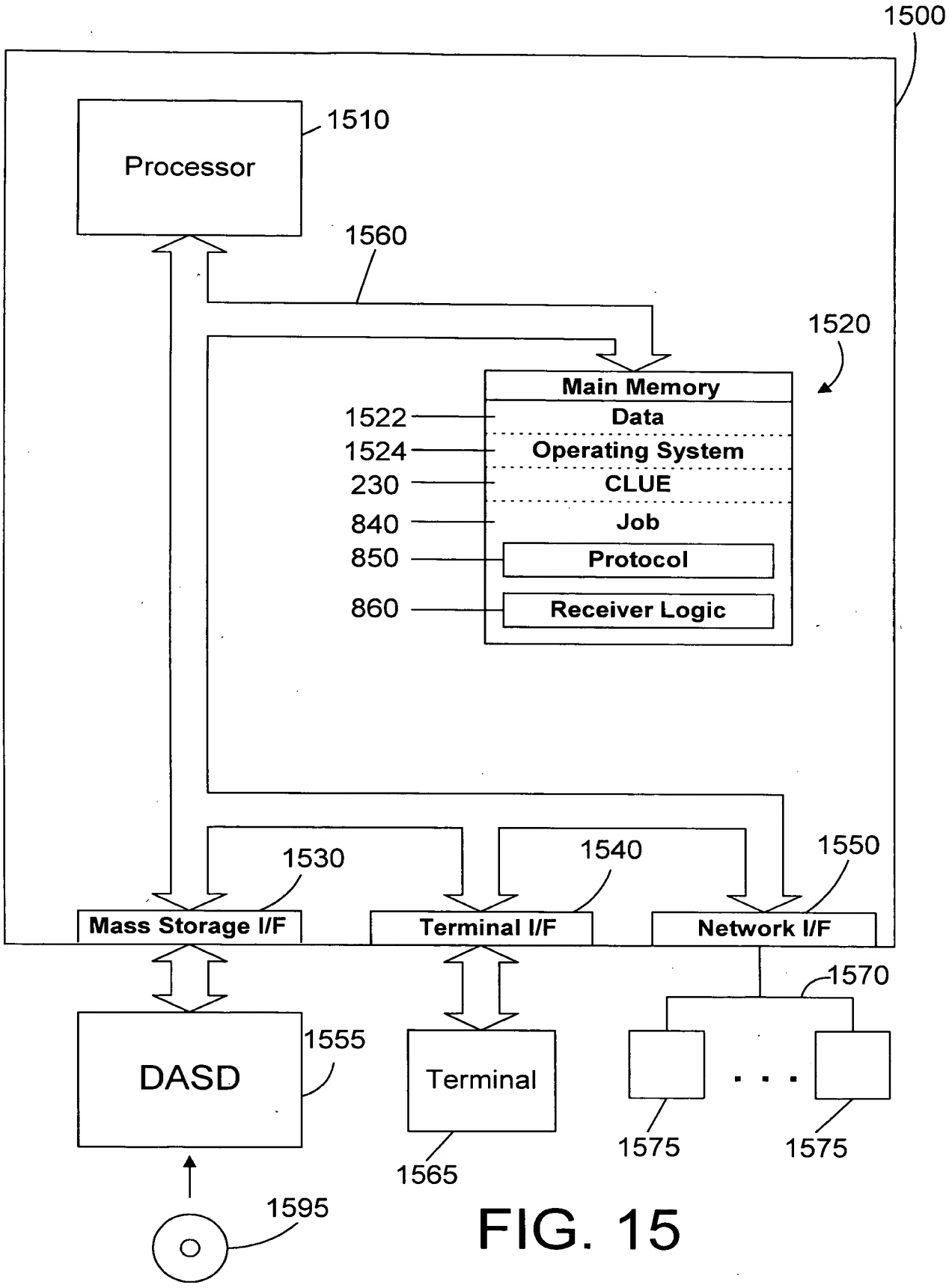
1500
Processor
1510
1560
1520
Main Memory
1522
Data
1524
Operating System
230
CLUE
840
Job
850
Protocol
860
Receiver Logic
1530
1540
1550
Mass Storage I/F
Terminal I/F
Network I/F
1570
DASD
1555
Terminal
1565
1575
1575
1595

FIG. 15